MOSTEK®

Z80 MICROCOMPUTER SYSTEMS

Operations Manual

RAM-80BE MEMORY EXPANSION BOARD

MEMORY EXPANSION BOARD (RAM-80BE)

(MK78110)

OPERATIONS MANUAL

MK78555

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SECTION 1

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. The RAM-80BE shown in Figure 1-1 provides a low cost means of expanding RAM and parallel I/O for a Z80 microcomputer system. The RAM-80BE is a peripheral board which can be directly interfaced to the MOSTEK Z80 Software Development Board (SDB-80E) or any Z80 Microprocessor based system.

1-3. GENERAL DESCRIPTION.

1-4. FUNCTIONAL. The RAM-80BE is a combination memory and I/O expansion board. The memory may be configured to have a memory capacity of 16K, 32K, 48K, or 65K bytes of RAM. This on-board memory expandability is made possible by population options of either eight, sixteen, twenty-four or thirty-two MK4116-4 (16,384x1 MOS dynamic RAM) memories. The RAM-80BE provides strapping options for positioning the decoded memory space to start on any 16K address boundary. In addition to the add-on memory, the RAM-80BE provides four 8-bit I/O ports from the two on-board MK3881 Z80 PIO circuits. Each I/O port is fully TTL buffered and has two handshake lines per I/O port. The RAM-80BE also includes logic for a "Page Mode Operation" which permits up to 1 mega-byte (sixteen 65Kx8 RAM-80BEs) to be used in a single SDB-80E system.

1-5. PHYSICAL. The RAM-80BE is implemented on a double Eurocard printed circuit board. The board requires three DC voltages at levels of +5, +12, and -12 VDC. The RAM-80BE is interfaced to a system by connectors SK1 and SK2.

1-6. SPECIFICATIONS.

1-7. Table 1-1 lists nomenclature and part numbers for the RAM-80BE and its accessories. Table 1-2 lists the overall specifications for the RAM-80BE. Table 1-3 lists the pin usage of connectors SK1 and SK2.

Figure 1-1. RAM-80BE Board.

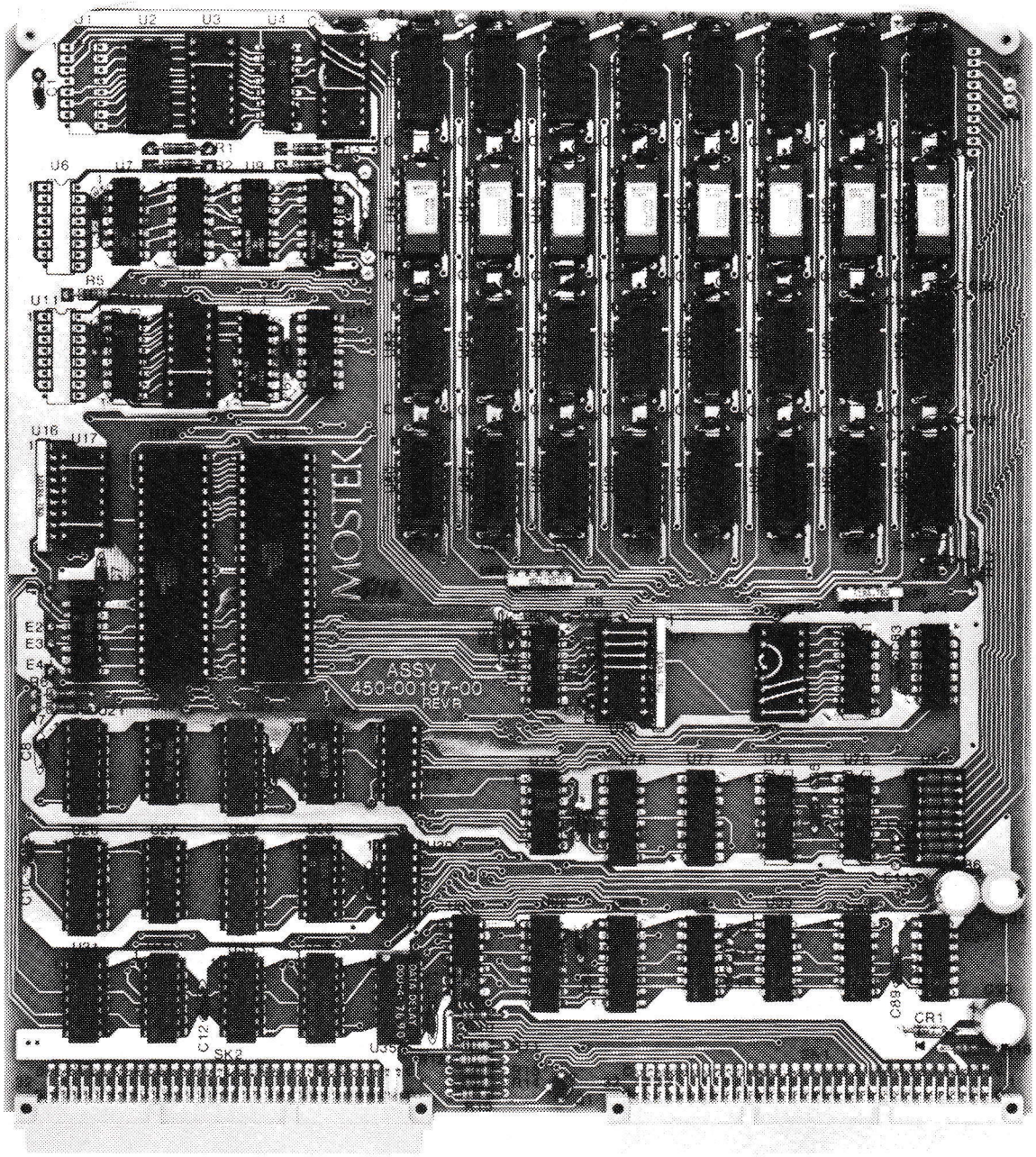


Table 1-1. Available Items

NAME	DESCRIPTION	PART NO
RAM-80BE	Expandable 16,384 byte RAM board with 8-MK4116s, sockets for 24 additional MK4116s, 2-MK3881 Z80 PIOs, plus page mode capability.	MK78110
XRAM-80B**	RAM-80BE Expansion Package, includes 8-MK4116 RAMs for insertion in the RAM-80BE board plus a blank strapping header and documentation.	MK78126

** The XRAM-80B package is available to RAM-80BE customers only. It is therefore required that each order for an XRAM-80B be accompanied by an Authorization Certificate from the RAM-80BE package. (Each RAM-80BE package is shipped with three of these non-transferable, non-replaceable certificates.)

Table 1-2. Specifications.

Memory Capacity	Up to 65,536 bytes
Memory Access	345 ns max.
Memory Cycle	450 ns min.
Parallel I/O	Four 8-bit ports w/handshake lines
Interface levels	TTL compatible
	+12 VDC +_ 5%, 200 mA (typ); 575 mA (max)
	-12 VDC +_ 5%, 25 mA (typ); 30 mA (max)
	+5 VDC +_ 5%, 1.1A (typ); 1.5 A (max)
Physical Dimensions	250 mm x 233.4 mm x 18 mm
Operating Temperature	0 C to 50 C

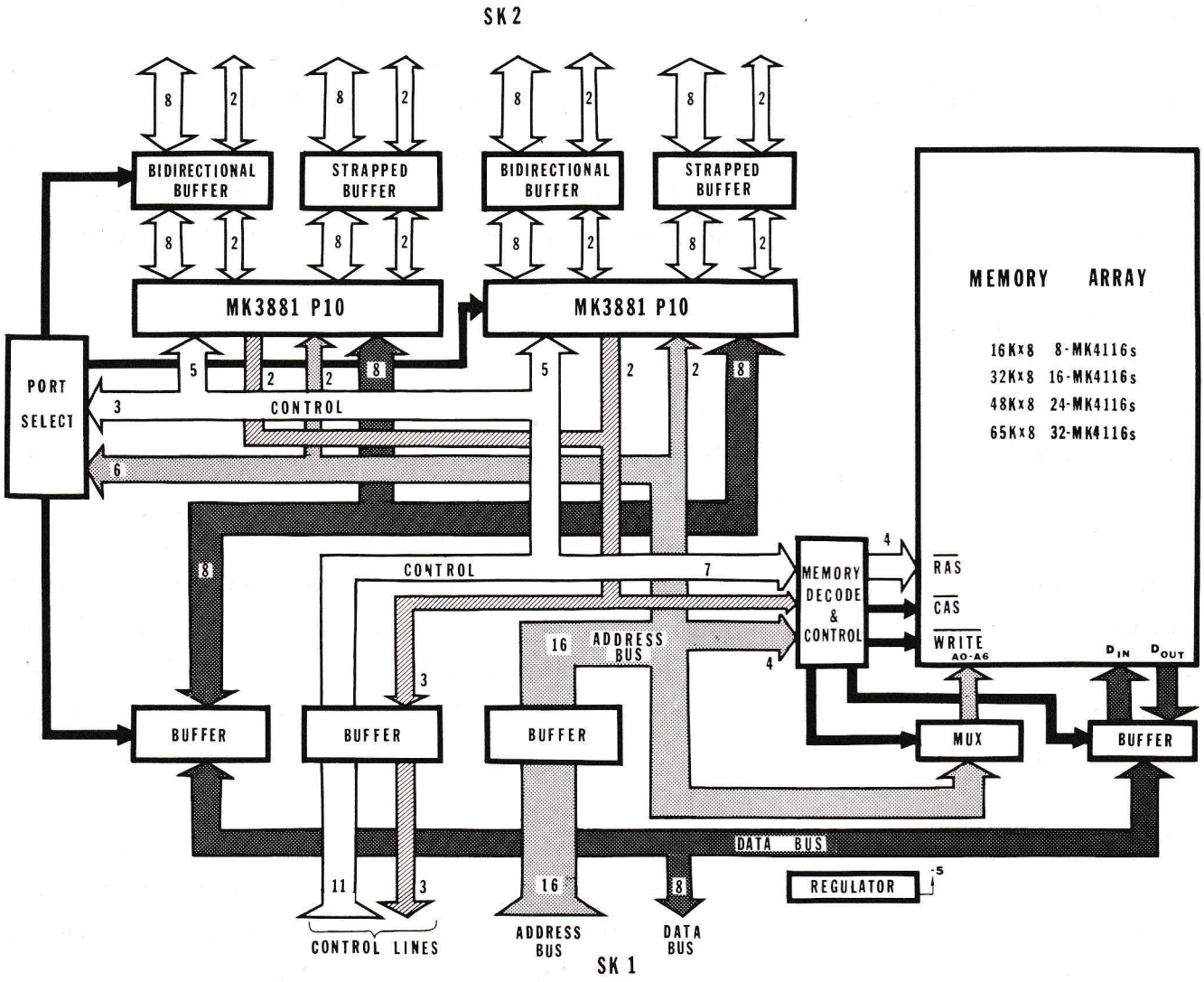
Table 1-3. Connector SK1 and SK2 Pin Out.

SK1			SK2		
a		c	a		c
GND	1	GND	GND	1	GND
GND	2	GND	GND	2	GND
-12V	3	-12V		3	
+5V	4	+5V		4	
+5V	5	+5V		5	
+12V	6	+12V			
	7				
IEOB	8	IEIB			
BAO	9	$\overline{\text{BAI}}$			
	10	$\overline{\text{MEMDIS2}}$			
$\overline{\text{RESETB}}$	11	$\overline{\text{MEMDISB}}$	RDY2B	11	$\overline{\text{STB2B}}$
	12	M1B	P(D6)4	12	P(D6)3
$\overline{\text{MREQB}}$	13		P(D6)5	13	P(D6)2
	14		P(D6)6	14	P(D6)1
$\overline{\text{INTB}}$	15		P(D6)7	15	P(D6)0
	16	$\overline{\text{RDB}}$	RDY2A	16	$\overline{\text{STB2A}}$
DB	17	AOB	P(D4)4	17	P(D4)3
$\overline{\text{IORQB}}$	18	A1B	P(D4)5	18	P(D4)2
$\overline{\text{WRB}}$	19	A2B	P(D4)6	19	P(D4)1
$\overline{\text{RFSHB}}$	20	A3B	P(D4)7	20	P(D4)0
	21	A4B		21	
$\overline{\text{DINB}}$	22	A5B		22	
	23	A6B	RDY1B	23	STB1B
	24	A7B	P(D2)4	24	P(D2)3
$\overline{\text{DOB}}$	25	A8B	P(D2)5	25	P(D2)2

Table 1-3. Connector SK1 and SK2 Pin Out (Cont'd)

SK1			SK2		
a		c	a		c
D1B	26	A9B	P(D2)6	26	P(D2)1
D2B	27	A10B	P(D2)7	27	P(D2)0
D3B	28	A11B	RDY1A	28	$\overline{\text{STB1A}}$
D4B	29	A12B	P(DO)4	29	P(DO)3
D5B	30	A13B	P(DO)5	30	P(DO)2
D6B	31	A14B	P(DO)6	31	P(DO)1
D7B	32	A15B	P(DO)7	32	P(DO)0

Figure 2-1. FUNCTIONAL BLOCK DIAGRAM.



2-9. PARALLEL I/O INTERFACE.

2-10. The following functions from Figure 2-1 make up the RAM-80BE parallel interface: MK3881 PIO's, port select, bidirectional buffers, strapped buffers, data buffers and control buffers.

2-11. MK3881 PIO's. The MK3881 parallel input/output device is the central part of the PIO interface. The PIO provides two 8-bit ports with two handshake lines per port.

2-12. PORT SELECT. The port select function is responsible for selecting one of the PIO's if the selected port address and the appropriate control signals are present. The port select is also used to select one port for the page mode circuit, if the page mode is being used.

2-13. BIDIRECTIONAL BUFFERS. The bidirectional buffers are connected to port A of the PIO's and can be used as either an input, output, or bidirectional tri-state 8-bit port. The bidirectional buffers are configured by the use of jumpers contained on DIP headers. Strapping of the jumpers is illustrated in the utilization section.

2-14. STRAPPED BUFFERS. The strapped buffers are connected to port B of the PIO's and can be used as either an input or an output port. Furthermore, the port may be divided into two four bit sections, with one section an input, and one section an output. Options for the strapped buffers are shown in the utilization section.

2-15. DATA AND CONTROL BUFFERS. The data and control buffers, isolate the data bus and the control bus from the PIO's.

SECTION 3

UTILIZATION

3-1. INTRODUCTION.

3-2. This section will explain the various options for the memory and parallel I/O sections of the RAM-80BE.

3-3. PARALLEL INTERFACE.

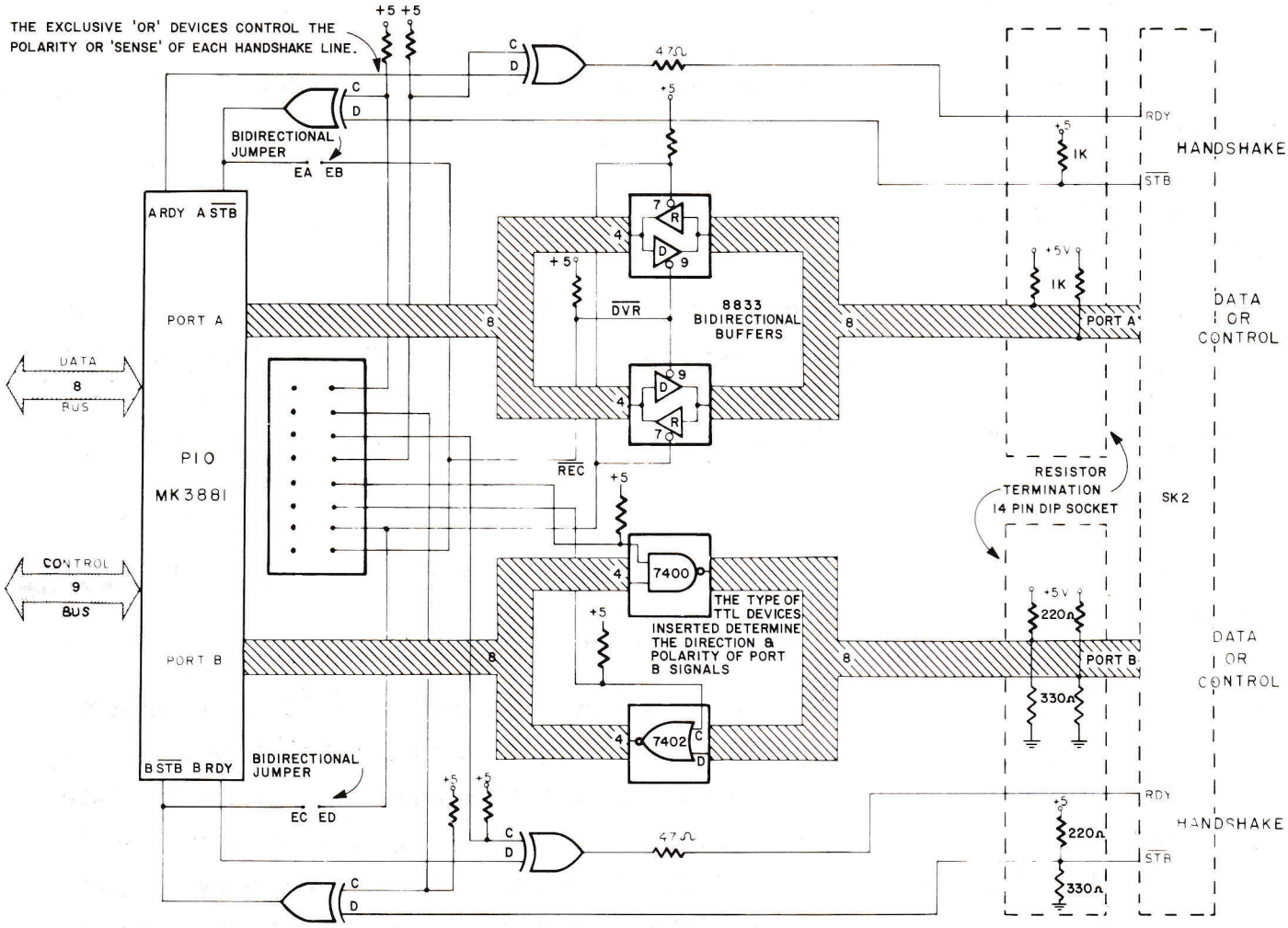
3-4. Two Parallel I/O Controllers (MK3881) are included on the RAM-80BE. This gives four independent 8-bit I/O ports with two handshake (data transfer) control lines per port. All I/O lines are TTL buffered and have provision for termination resistors on board. Figure 3-1 shows a diagram of a generalized parallel I/O port.

3-5. CONNECTOR. Connector SK2 is used for I/O and is identified as Parallel I/O#1 and Parallel I/O#2.

3-6. RESISTOR TERMINATIONS. One 14-pin socket per port is provided for resistor dual inline packages so that terminations may be placed on the data lines. A parallel termination is provided for each 8-bit port data line plus the input strobe (STB) handshake line. As shown in Figure 3-1, the termination resistors may be either simple pull up resistors (port A) or an impedance matching network (port B). The RAM-80BE is shipped with four 1KLpull up terminations. In addition to the parallel termination resistors each ready (RDY) handshake output line is "terminated" with a series 47Lresistor on the board. This is used to help damp and reduce any reflections on this output line.

3-7. HANDSHAKE LINE BUFFERS (STB, RDY). Standard TTL Exclusive OR gates (7486) are used to buffer and isolate these lines. Jumper options (located on the Jumper Select Header) are provided on board to independently control the polarity or "sense" of each handshake signal so as to ease the interfacing between the board and peripheral devices. The input Control and Data lines to each gate are marked

Figure 3-1. GENERALIZED PARALLEL I/O INTERFACE.



C and D respectively in Figure 3-1 controls the data as shown:

Control = logic "0"; Data = non-inverted

Control = logic "1"; Data = inverted

Table 3-1. indicates how the handshake buffers are jumpered on the RAM-80BE as shipped from the factory.

Table 3-1. Strapping of Handshake Buffers as Shipped From Factory

	DATA LINE	POLARITY OF BUFFER
PIO # 1	A RDY	inverting
	A STB	inverting
	B RDY	inverting
	B STB	non-inverting
PIO # 2	A RDY	non-inverting
	A STB	non-inverting
	B RDY	non-inverting
	B STB	non-inverting

3-8. PORT A DATA BUFFER. Port A data bus lines are buffered using two quad party line non-inverting transceivers (DS8833). This allows true bidirectional capability. Jumper options allow for fixed IN, fixed OUT or BIDIRECTIONAL under software control. Replacing the DS8833 with a DS8835 effects a polarity change in the output bits. The drivers and receiver (as designated by D and R respectively) in Figure 3-1 are enabled by jumpers on the Jumper Select Header and on two sets of Wire Wrap pins (E A-B, E C-D). The enable lines are listed as REC for receiver enable and DVR for driver enable. The jumper connections will be detailed later under Header and Jumper Information.

3-9. PORT B DATA BUFFERS. Port B data lines are arranged in such a fashion (in increments of 4-bit sections) as to allow the user to determine the port direction. Sockets are provided for standard 14-pin 7400 series TTL packages. Depending upon the package type inserted, the port may be dedicated IN or OUT.

In the output mode ports may be selected to provide standard, or buffered drive, active pull ups or open collector, low or high voltage, etc. Figure 3-1. shows an arbitrary arrangement whereby four bits are buffered OUT by a 7400 NAND gate while four bits are buffered IN by 7402 NOR gate. The Data Control lines of these gates are marked D and C respectively. The control line for a NAND gate will be pulled high by the pull up resistor, the control line for a NOR gate needs to be pulled low, while the control line for an Exclusive - or gate will determine the output polarity. Table 3-2. shows the different types of devices that may be used to buffer port B.

Table 3-2. Device Options for Port B.

IN	OUT
7402 STD drive, inverting (NOR)	7400 STD drive, inverting (NAND) 7403 open collector, inverting (NAND) 7408 STD drive, non-inverting (AND) 7409 open collector, non-inverting (AND) 7426 open collector, high-voltage, inverting (NAND) 7432 STD drive, non-inverting (OR) 7437 buffer, inverting (NAND) 7438 open collector, buffer, inverting (NAND) 7486 STD drive, Invert/non-inverting (EX-OR)

3-10. HEADER AND JUMPER INFORMATION. Headers U17 (for I/O #1) and U70 (for I/O #2) contain the following jumper options:

1) Determine polarity of handshake lines by strapping the control line of the Exclusive OR buffers U20 and U69.
2) Strap the control line on the buffers of port B for proper AND, NOR, or EX-OR operation.
3) Enable the Receiver or Driver portions of the port A buffers.

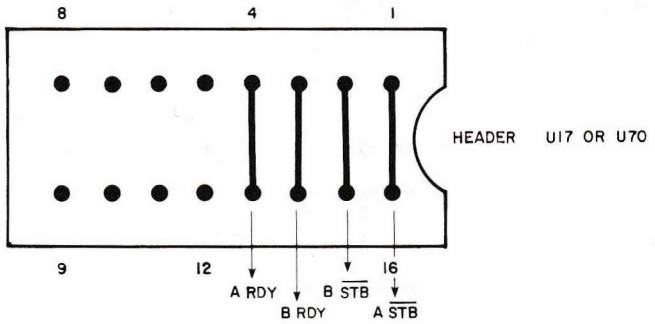
Figure 3-2. shows the header and Wire Wrap pins jumpered so that each control line is strapped to logical "0". Table 3-3, 3-4 and 3-5 summarize all jumper options for the two I/O interfaces. Refer to Figure 3-3 and 3-4 which show the electrical configuration of each interface as shipped from the factory for a RAM-80BE.

Table 3-3. Jumper Options for Handshake Buffers.

Designator		Header and Jumper Pins
PIO #1	A RDY	U17
	INVERTED	Pin 4,13 OPEN
	NON-INVERTED	Pin 4,13 STRAPPED
	A STB	U17
	INVERTED	Pin 1,16 OPEN
	NON-INVERTED	Pin 1,16 STRAPPED
	B RDY	U17
	INVERTED	Pin 3,14 OPEN
	NON-INVERTED	Pin 3,14 STRAPPED
	B STB	U17
	INVERTED	Pin 2,15 OPEN
	NON-INVERTED	Pin 2,15 STRAPPED
PIO #2	A RDY	U70
	INVERTED	Pin 4,13 OPEN
	NON-INVERTED	Pin 4,13 STRAPPED
	A STB	U70
	INVERTED	Pin 1,16 OPEN
	NON-INVERTED	Pin 1,16 STRAPPED
	B RDY	U70
	INVERTED	Pin 3,14 OPEN
	NON-INVERTED	Pin 3,14 STRAPPED
	B STB	U70
	INVERTED	Pin 2,15 OPEN
	NON-INVERTED	Pin 2,15 STRAPPED

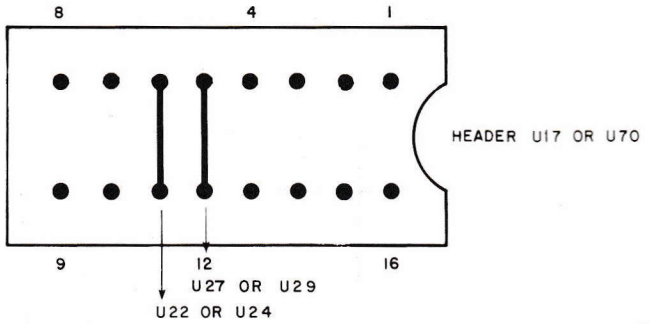
Figure 3-2. STRAPS TO CONTROL PARALLEL PORTS.

A.



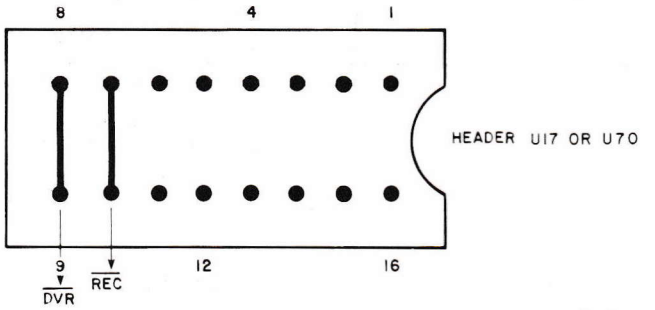
CONTROL LINE FOR EACH HANDSHAKE BUFFER IS STRAPPED TO A LOGIC "0" SO HANDSHAKE DATA IS NON-INVERTED. ABSENCE OF A STRAP INVERTS THE DATA.

B.



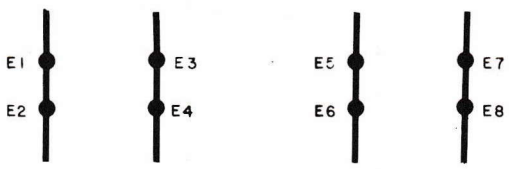
CONTROL LINE FOR EACH HANDSHAKE BUFFER IS STRAPPED TO A LOGIC "0" SO THAT THE 'OR' OR 'NOR' BUFFER IS ENABLED. ADDITION OF A STRAP APPLIES TO A 'AND','NOR' OR POSSIBLY AN EX 'OR' GATE.

C.



BOTH THE RECEIVER AND DRIVER CONTROL LINES ARE STRAPPED TO "0" CAUSING THE RECEIVERS AND DRIVERS TO BE ENABLED. IN OPERATION EITHER ONE MAY BE STRAPPED BUT NOT BOTH. IN THE BIDIRECTIONAL MODE NO STRAP IS USED.

D.



WIRE WRAP PINS ARE WIRED FOR BIDIRECTIONAL MODE.

Table 3-4. Jumper Options for Port B Control Lines.

BUFFER AND SOCKET	HEADER AND JUMPERS
7400, 7403, 7408, 7409 7426, 7437, 7438	
U27	U17 Pin 5,12 OPEN
U22	U17 Pin 6,11 OPEN
U29	U70 Pin 5,12 OPEN
U24	U70 Pin 6,11 OPEN
7402, 7432	
U27	U17 Pin 5,12 STRAPPED
U22	U17 Pin 6,11 STRAPPED
U29	U70 Pin 5,12 STRAPPED
U24	U70 Pin 6,11 STRAPPED
7486	
U27 (INVERTING)	U17 Pin 5,12 OPEN
U27 (NON-INVERTING)	U17 Pin 5,12 STRAPPED
U22 (INVERTING)	U17 Pin 6,11 OPEN
U22 (NON-INVERTING)	U17 Pin 6,11 STRAPPED
U29 (INVERTING)	U70 Pin 5,12 OPEN
U29 (NON-INVERTING)	U70 Pin 5,12 STRAPPED
U24 (INVERTING)	U70 Pin 6,11 OPEN
U24 (NON-INVERTING)	U70 Pin 6,11 STRAPPED

Two blank schematics (Figures 3-5 and 3-6) of interfaces #1 and #2 are included to help the user effect any changes in the port options.

Table 3-5. Jumper Options for Port A Control Lines

DIRECTION	SOCKET	HEADER & JUMPERS	WIRE WRAP PINS
INPUT	U21, U26 PIO#1	U17 Pin 7,10 STRAPPED U17 Pin 8,9 OPEN	E 1-2 OPEN E 3-4 OPEN
	U23, U28 PIO#2	U70 Pin 7,10 STRAPPED U70 Pin 8,9 OPEN	E 5-6 OPEN E 7-8 OPEN
OUTPUT	U21, U26 PIO#1	U17 Pin 7,10 OPEN U17 Pin 8,9 STRAPPED	E 1-2 OPEN E 3-4 OPEN
	U23, U28 PIO#2	U70 Pin 7,10 OPEN U70 Pin 8,9 STRAPPED	E 5-6 OPEN E 7-8 OPEN
BI-DIRECTIONAL	U21, U26 PIO#1	U17 Pin 7,10 OPEN U17 Pin 8,9 OPEN	E 1-2 CONNECTED E 3-4 CONNECTED
	U23, U28 PIO #2	U70 Pin 7,10 OPEN U70 Pin 8,9 OPEN	E 5-6 CONNECTED E 7-8 CONNECTED

3-11. PORT ADDRESSES. Each port in a PIO chip has two addresses; one for CONTROL and one for DATA. The port addresses are derived from the lowest 8-address lines (A0-A7). A0 and A1 are fed directly to the PIO so that A0 selects either control or data and A1 selects either port A or port B. The rest of the addresses, A2 - A7 are decoded in the port section which provides a chip enable for each PIO. The CE function, along with A0 and A1, create the proper address for each port. PIO#1 and PIO#2 may be assigned to any one of the 4 port address segments within Block #1 or Block #2. However, PIO#1 and PIO#2 must reside within the same block. See Table 3-6.

Figure 3-3. PARALLEL I/O INTERFACE #1 AS SHIPPED FROM FACTORY.

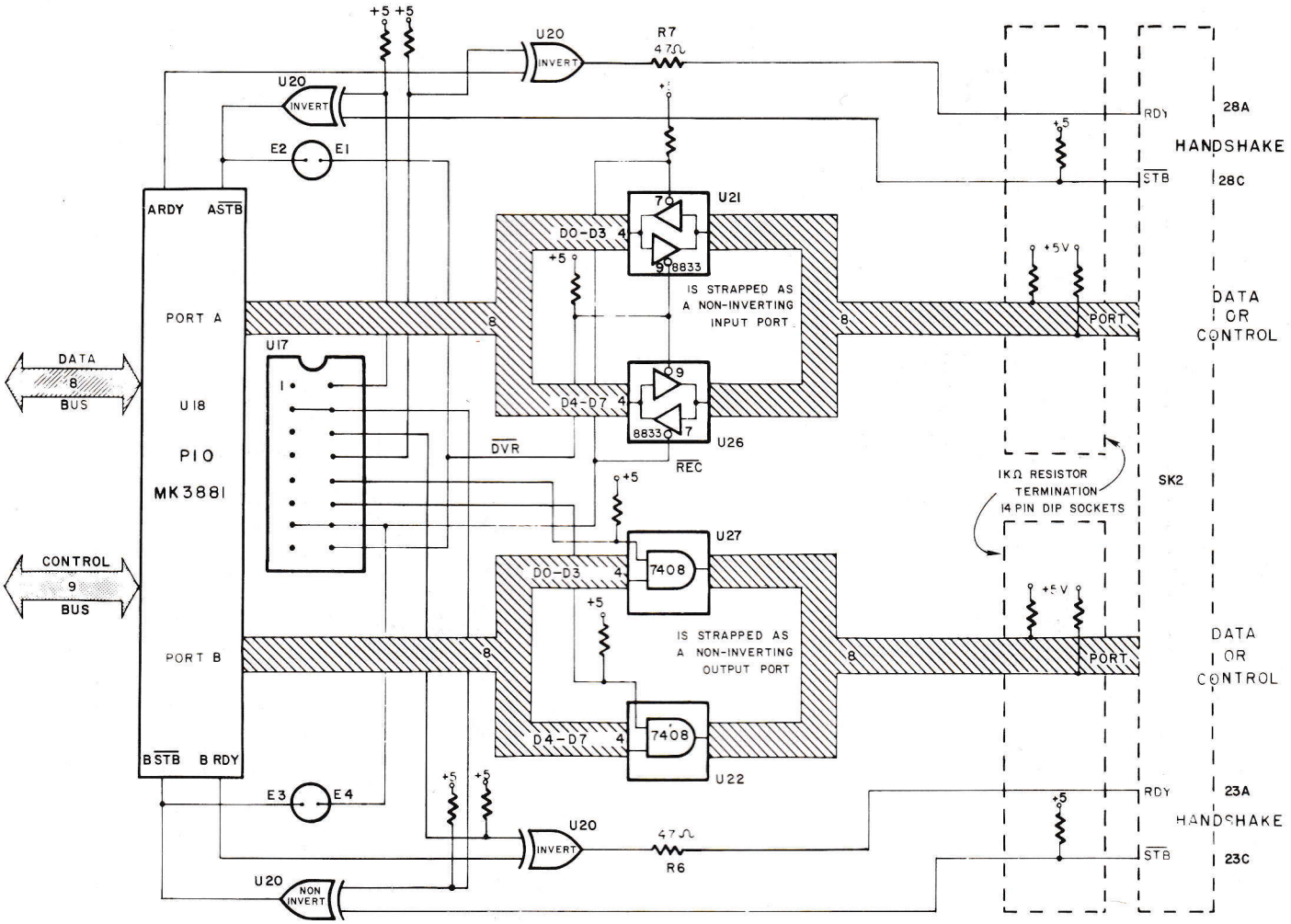


Figure 3-4. PARALLEL I/O INTERFACE #2 AS SHIPPED FROM FACTORY.

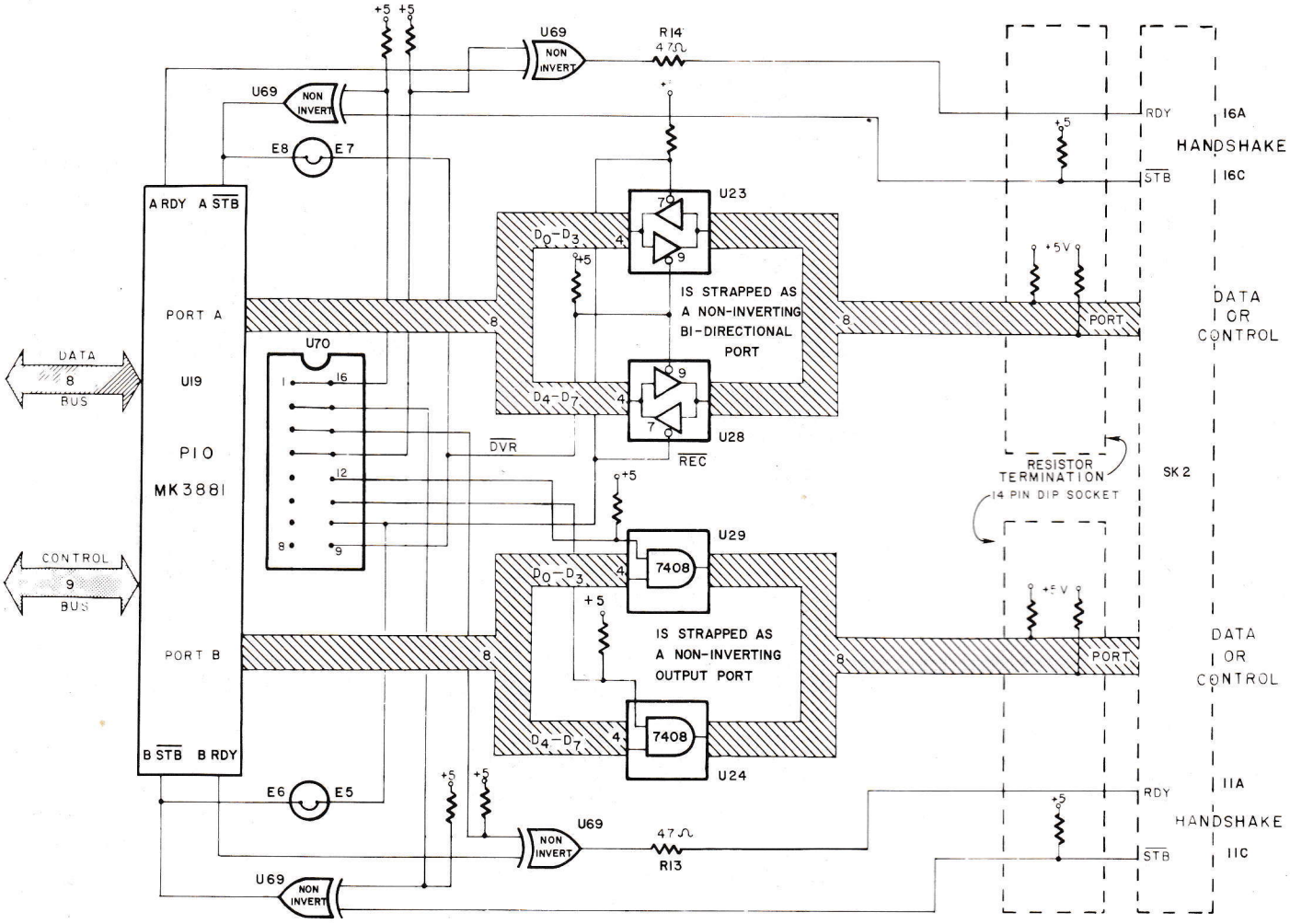


Figure 3-5. PARALLEL I/O INTERFACE.

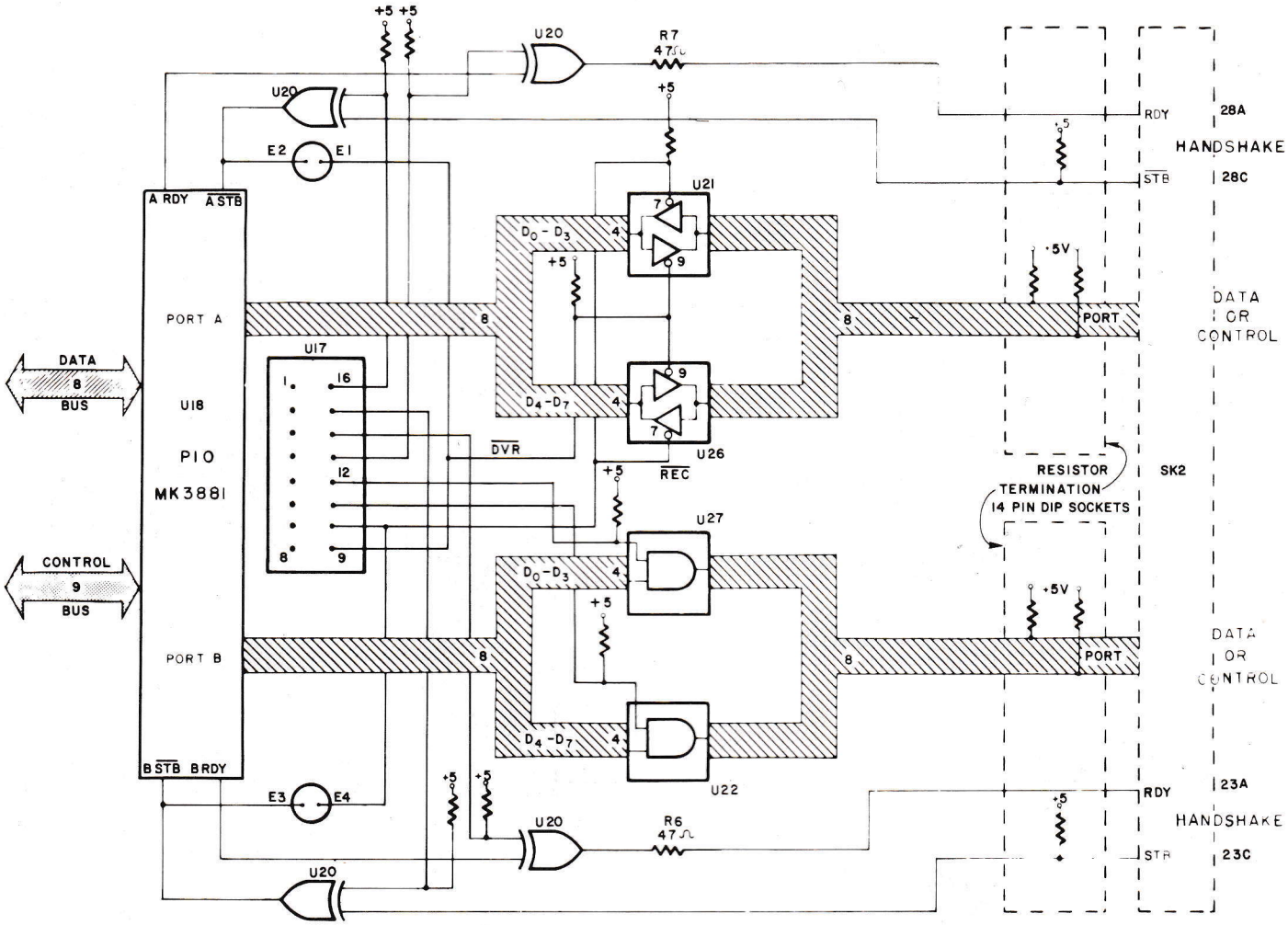
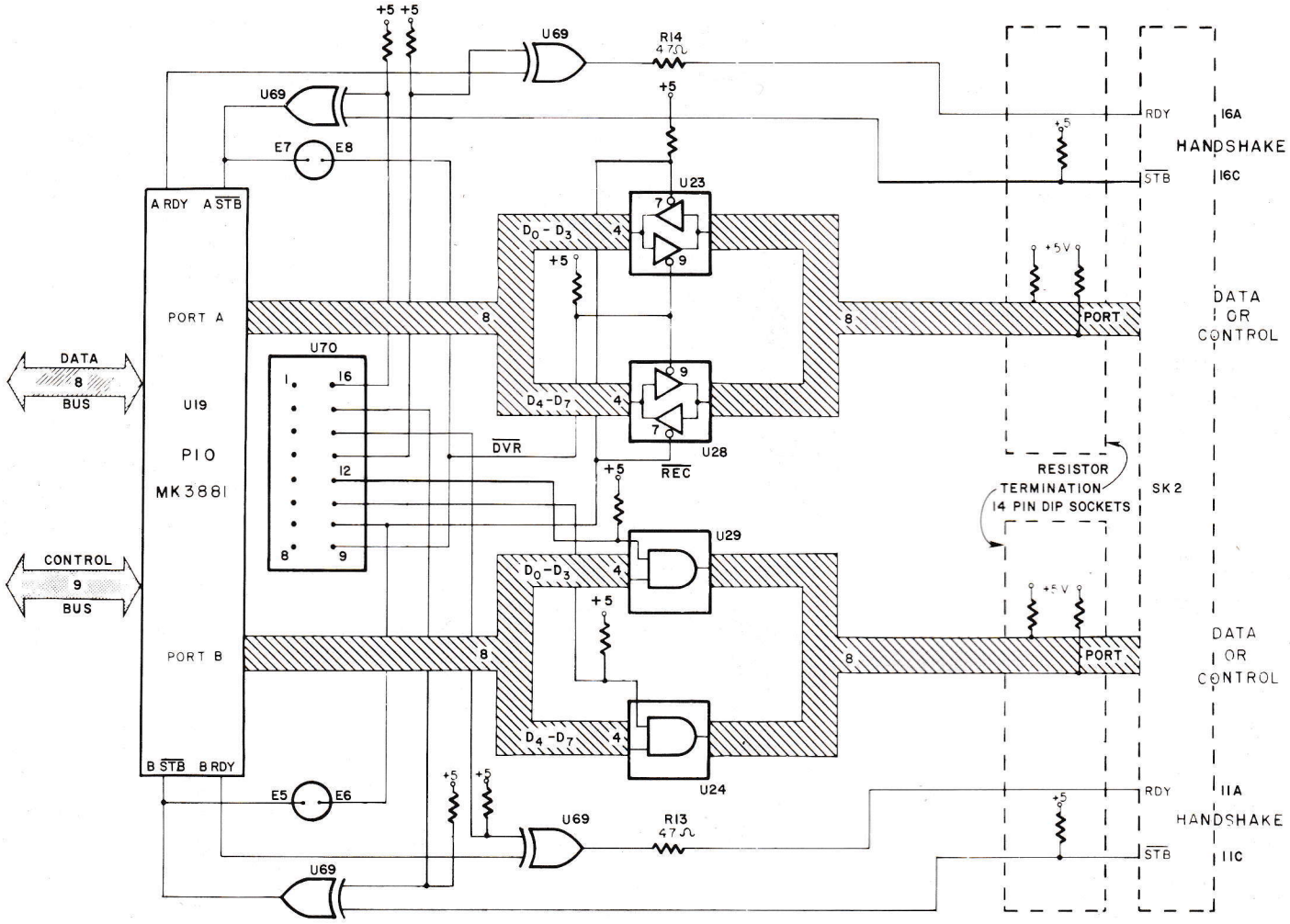


Figure 3-6. PARALLEL I/O INTERFACE.



If page mode is used, one port segment will be used for control of the page mode circuitry.

Table 3-6. Decoded Port Available for PIO#1, PIO#2, and Page Mode.

BLOCK #1	BLOCK #2
A0 - A3	60-63
A4 - A7	64-67
A8 - AB	68-6B
AC - AF	6C-6F
B0 - B3	70-73
B4 - B7	74-77
B8 - BB	78-7B
BC - BF	7C-7F

3-12. HEADER AND JUMPER INFORMATION. Header U72 is used for the following jumper options:

1) Set ports for PIO#1, PIO#2 and page mode.
2) Determine which block that ports will be selected from.

Figure 3-7 shows the header U72 and how it is strapped from factory.

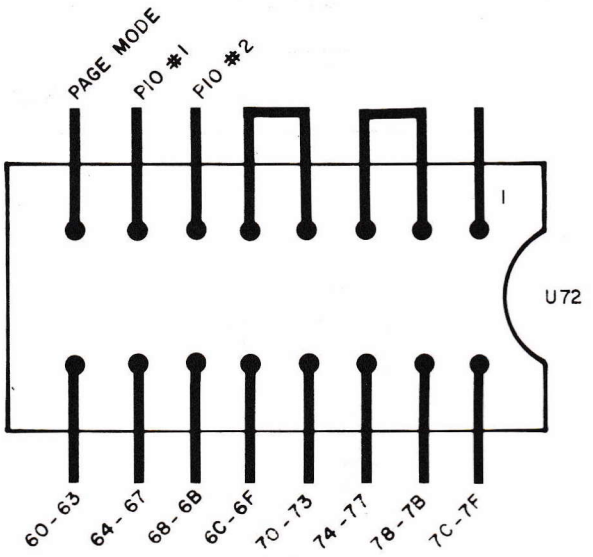
3-13. MEMORY INTERFACE

3-14. The RAM-80BE can be populated with 16K, 32K, 48K, or 64K bytes of RAM. This on-board memory expandability is made possible by population options of eight, sixteen, twenty-four or thirty-two MK4116-4 (16,384x1 MOS dynamic RAM) memories. The RAM-80BE, provides strapping options for positioning the decoded memory space to start start on any 16K address boundary. In addition to the add-on memory, the RAM-80BE provides logic to allow memory to be allocated into memory pages.

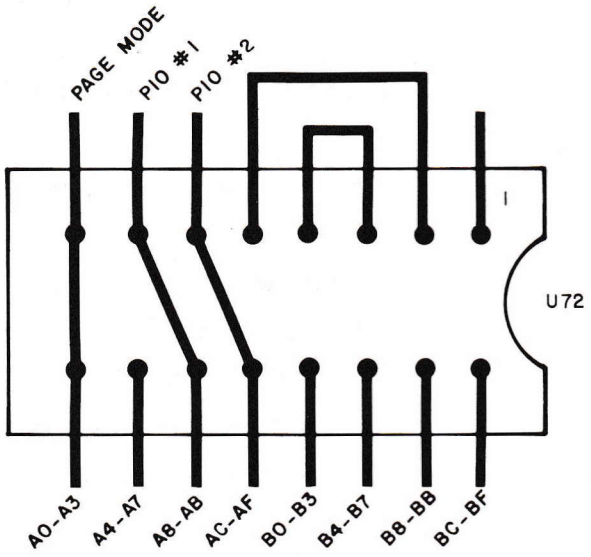
3-15. MEMORY DECODING JUMPERS. Decoding for each of the 16K segments is done by strapping options located on U13. Figure 3-9 shows the strapping options for U13, and how the board is strapped from the factory.

Figure 3-7. DECODED PORTS AVAILABLE FOR PIO #1, PIO #2, AND PAGE MODE

A.



B. *



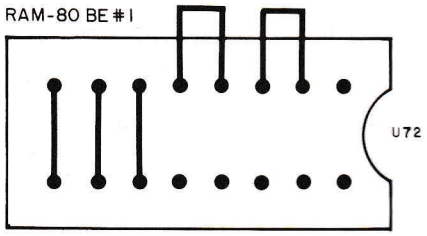
PORTS:

A0-A3	PAGE MODE
A8-AB	PIO # 1
AC-AF	PIO # 2

* SHIPPED FROM FACTORY IN THIS CONFIGURATION.

Figure 3-8. HEADER STRAPPING OPTIONS FOR PIO #1, PIO #2, AND PAGE MODE PORT SELECT

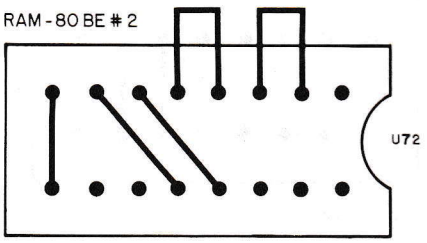
A.



PORTS:

60-63	PAGE MODE
64-67	PIO #1
68-6B	PIO #2

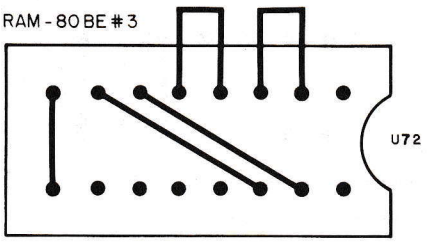
B.



PORTS:

60-63	PAGE MODE
6C-6F	PIO #1
70-73	PIO #2

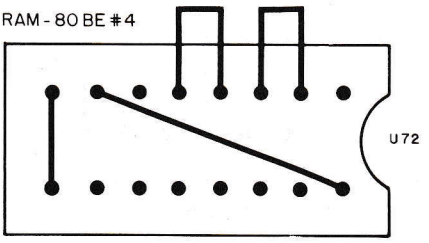
C.



PORTS:

60-63	PAGE MODE
74-77	PIO #1
78-7B	PIO #2

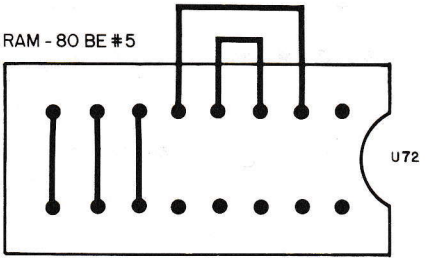
D.



PORTS:

60-63	PAGE MODE
7C-7F	PIO #1

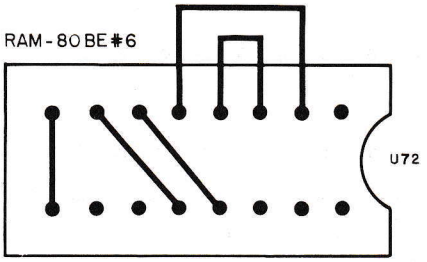
E.



PORTS:

A0-A3	PAGE MODE
A4-A7	PIO #1
A8-AB	PIO #2

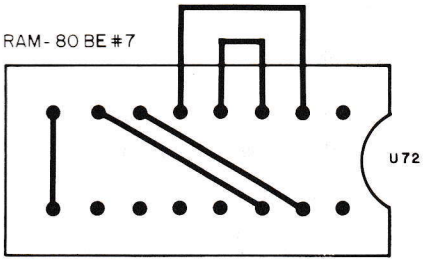
F.



PORTS:

A0-A3	PAGE MODE
AC-AF	PIO #1
B0-B3	PIO #2

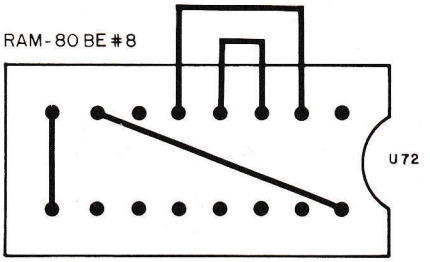
G.



PORTS:

A0-A3	PAGE MODE
B4-B7	PIO #1
B8-BB	PIO #2

H.

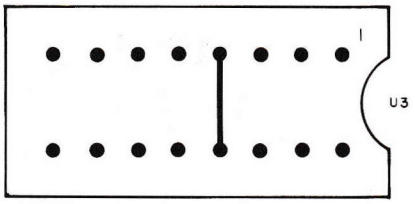


PORTS:

A0-A3	PAGE MODE
BC-BF	PIO #1

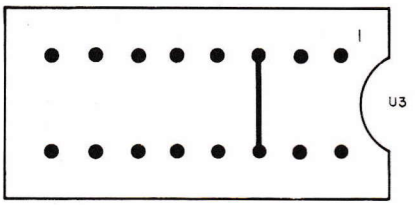
Figure 3-9. HEADER STRAPPING OPTIONS FOR POSITIONING RAM-80BE MEMORY

A.



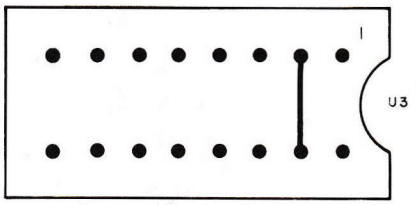
0 - 3FFF (16K BYTES)

B.



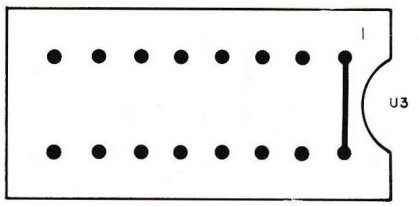
4000 - 7FFF (16K BYTES)

C.



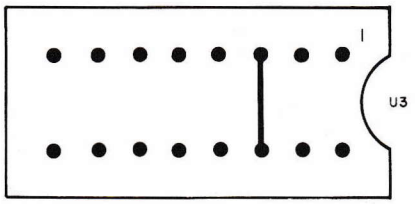
8000 - BFFF (16K BYTES)

D.



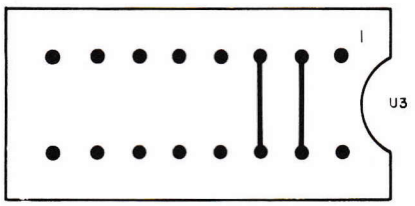
C000 - FFFF (16K BYTES)

E.*



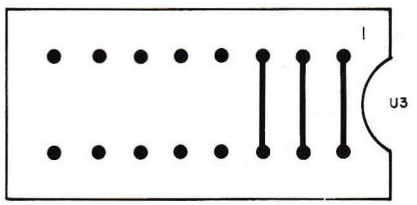
4000 - 7FFF (16K BYTES)

F.



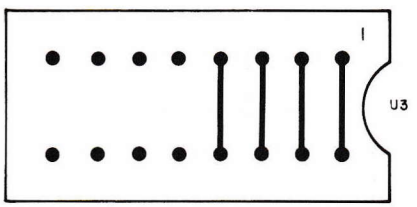
4000 - BFFF (32K BYTES)

G.



4000 - FFFF (48K BYTES)

H.



0 - FFFF (65K BYTES)

* SHIPPED FROM FACTORY IN THIS CONFIGURATION.

3-16. PAGE MODE. The RAM-80BE has a unique feature which allows the memory of the RAM-80BE to be used in a page mode. By using the page mode, the amount of RAM can be extended to a maximum of 16 RAM-80BE memory boards or 1 megabyte. (16 boards x 65,536 bytes per RAM-80BE) The amount of memory that can be present in a page is dependent upon the amount and location of memory on the SDB-80E. For example, if the SDB-80E is configured with 16Kx8 of memory that starts at 0000 and also has the ASMB-80 software package installed starting at C000H, the maximum memory that can be present on a RAM-80BE memory page is 32Kx8 or two rows of 16K RAMs, with origin at 4000H. Figure 3-10 shows an example of a typical page mode system using the SDB-80E and four RAM-80BE boards. The page mode for the RAM-80BE is implemented by using a latching output port that is fed into a 4 to 16 decoding circuit. To access a particular page of memory, the appropriate 4 bit code is output to all RAM-80BE memory boards via the selected I/O port.

NOTE: If more than eight RAM-80BE boards are used in a system, two I/O ports segments will be needed for the page mode.

See Figures 3-7 and 3-8. Whenever a power-on or manual reset is performed, the memory board residing in the page zero position will always be activated.

3-17. HEADER AND JUMPER INFORMATION. Headers U13 and U5 are used with page mode. Figure 3-11, 3-12 and 3-13 show the strapping for headers U13 and U5.

3-18. MEMORY DISABLE INPUTS. Two memory disable inputs are provided on the RAM-80BE for the purpose of inhibiting memory reads and memory writes on the board. The two signals are designated as $\overline{\text{MEMDIS}}$ and $\overline{\text{MEMDIS2}}$. $\overline{\text{MEMDIS}}$ is located on pin 11C of edge card connector SK1. A typical use for $\overline{\text{MEMDIS}}$ is to disable memory under control of the AIM-80E in-circuit-emulation card. $\overline{\text{MEMDIS2}}$ is located on pin 10C of edge card connector SK2 and is not used by the SDB-80E system. A typical use for $\overline{\text{MEMDIS2}}$ would be to disable memory on the RAM-80B by controlling $\overline{\text{MEMDIS2}}$ by external logic. Another use for MEMDIS2 would be to use the SDB-80E to disable RAM-80B memory when the SDB-80E was addressing memory on its board. This action would be necessary only if the RAM-80BE was populated with 48K or 65K bytes of memory. The memory disable signal from the SDB-80 would prevent memory decoding conflicts between the SDB-80E and the RAM-80BE. This modification consists of connecting a jumper wire from U47 pin 8 on the SDB-80E to pin 10C of SK1 on the SDB-80E. When this modification is made to the SDB-80E, SK1-10C will go

Figure 3-10. SDB-80E SYSTEM USING FOUR RAM-80BE's IN PAGE MODE

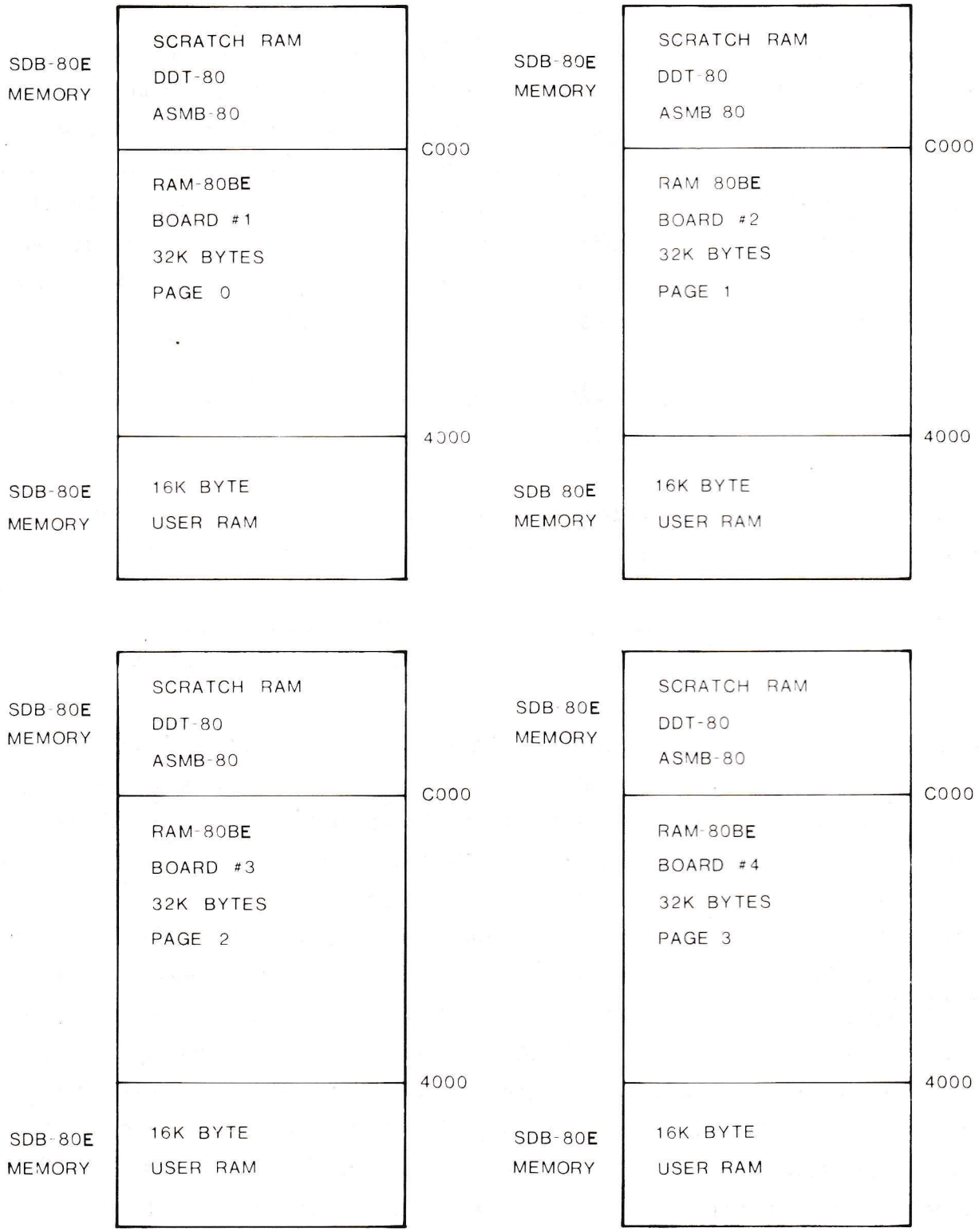
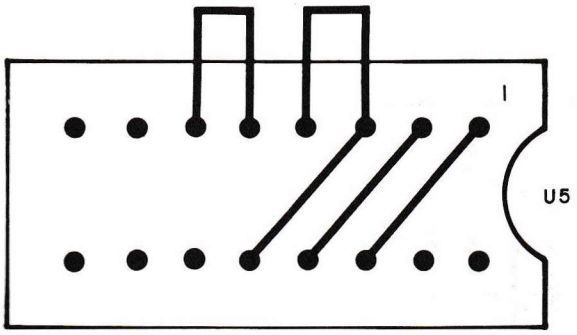


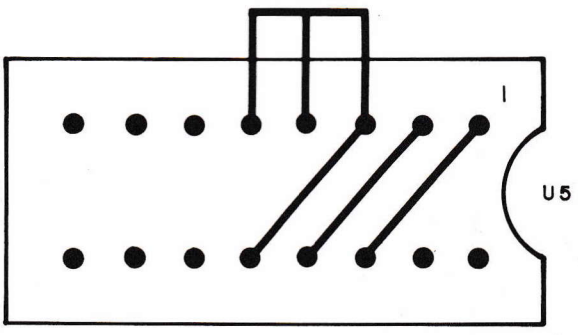
Figure 3-11. STRAPPING FOR ENABLING AND DISABLING PAGE MODE

A.



PIN 5 TO PIN 6 ENABLES PAGE MODE

B.*



PIN 5 TO PIN 3, 4, 12 DISABLES PAGE MODE

* SHIPPED FROM FACTORY IN THIS CONFIGURATION.

Figure 3-12. HEADER STRAPPING OPTIONS FOR PAGE SELECT 0-7.

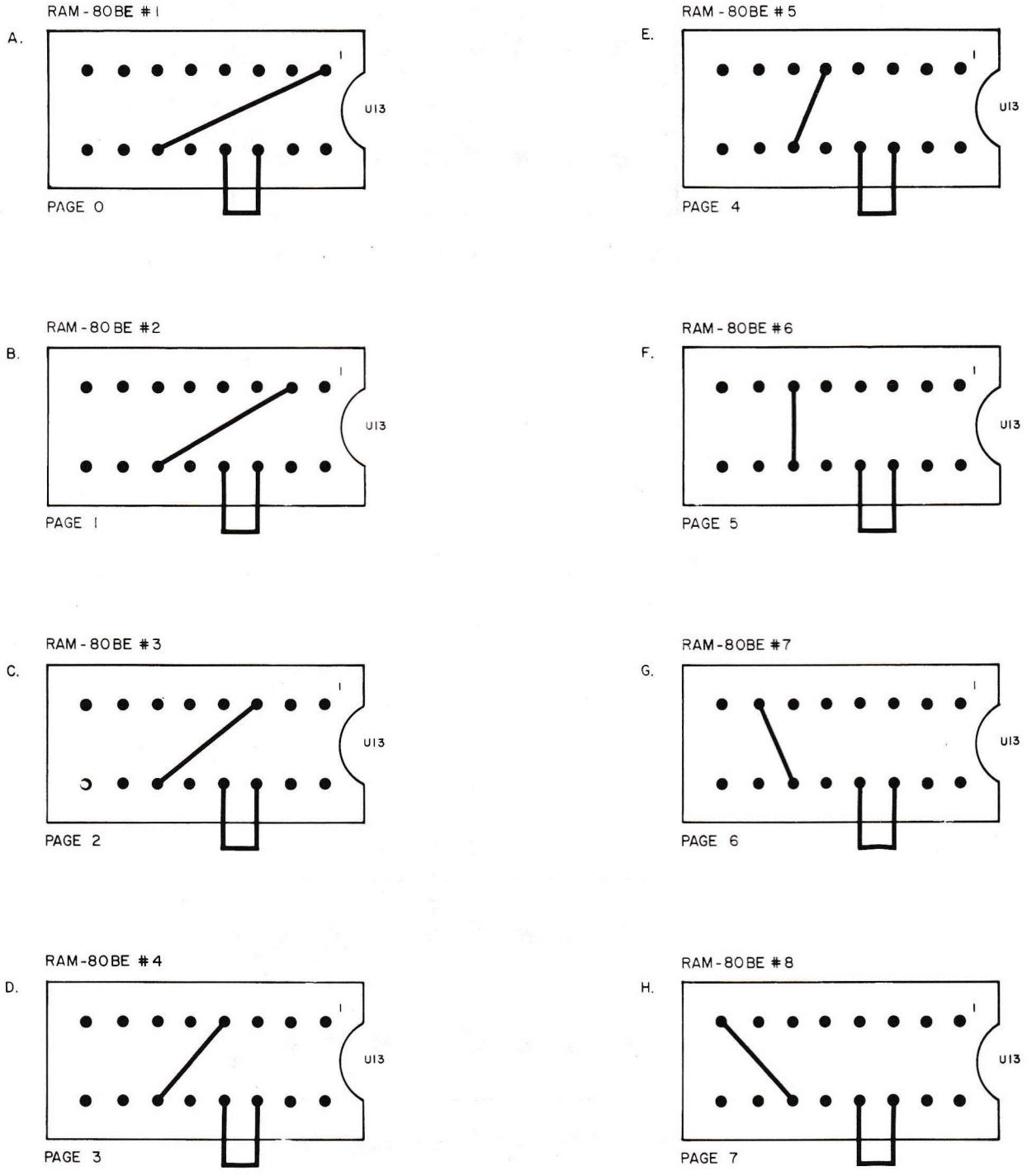
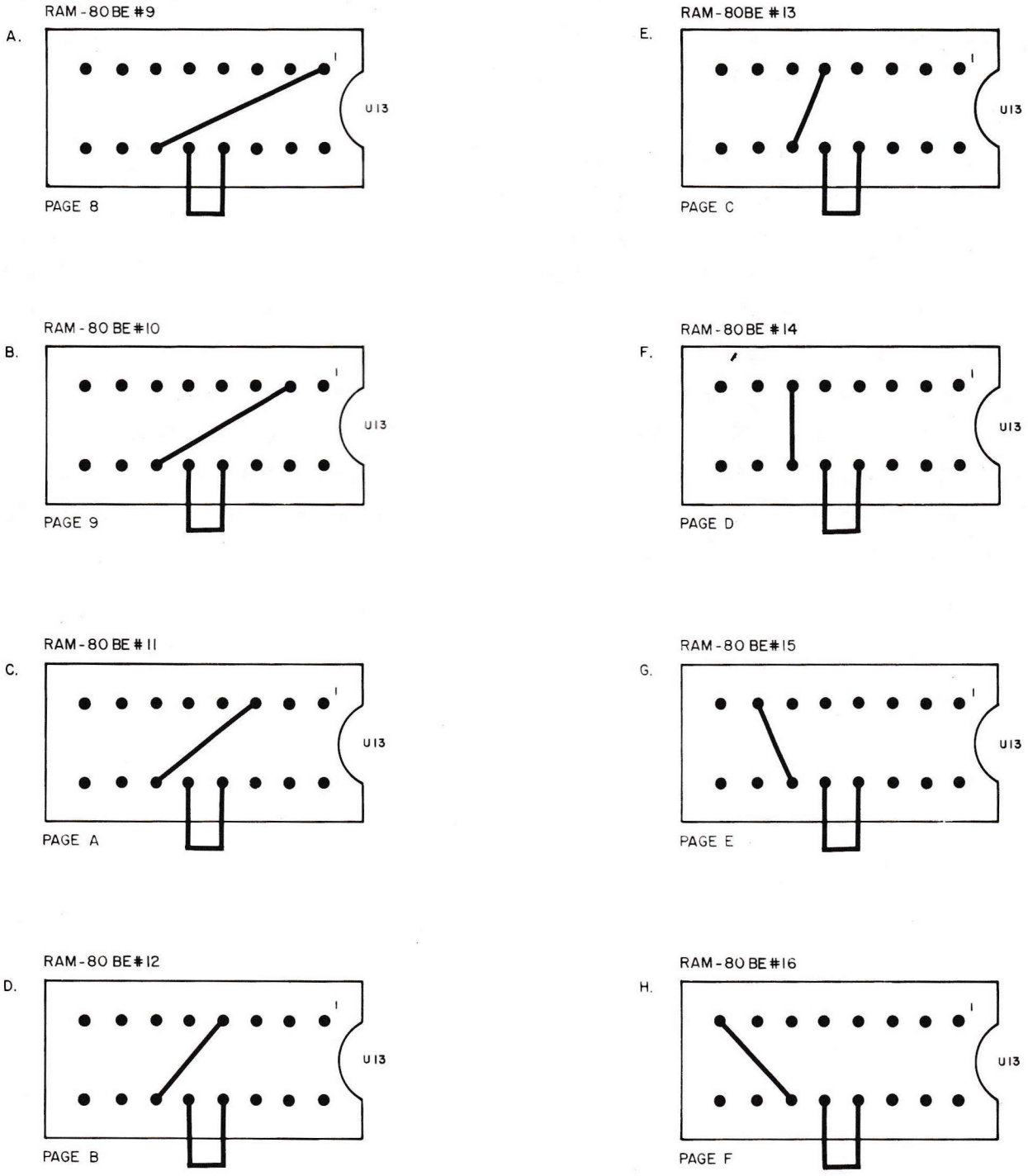


Figure 3-13. HEADER STRAPPING OPTIONS FOR PAGE SELECT 8-F.



low whenever memory is being addressed on the SDB-80E and will disable memory reads and memory writes on all RAM-80BE's in the system. Figure 3-14 shows a SDB-80E and RAM-80BE system with all memory on the SDB-80E disabled except the DDT-80 ROM and the scratch-pad RAM. With this configuration a fully populated RAM-80BE would have a total usable RAM of 63K (65K-2K-1K). This RAM could be extended beyond the 63K by using multiple RAM-80BE's in page mode.

3-19. ADDING MEMORY TO THE RAM-80BE USING THE XRAM-80B ADD ON MEMORY PACKAGE. Memory may be added to the RAM-80BE in 16K byte increments up to 65K bytes by using the XRAM-80B add-on memory package. The RAM-80BE is shipped from the factory with 16K bytes of memory starting at 4000H to 7FFFH. If the SDB-80E has 4K or 16K of RAM or the ASMB-80, DDT-80 software package is used, then sockets U36, U37, U38, U39, U40, U41, U42, U43 and U60, U61, U62, U63, U64, U65, U66, U67 cannot be populated on the RAM-80BE unless the memory disable signals on the SDB-80E and RAM-80BE are used to prevent memory decoding conflicts. Before installing memory in these sockets refer to the SDB-80E operations manual and paragraph 3-18 of this manual. Table 3-7 and Figure 3-9 show the jumpers and location of devices for adding memory to the RAM-80BE.

Figure 3-14. SDB-80E CONFIGURED TO DISABLE OVERLAPPING RAM-80BE MEMORY

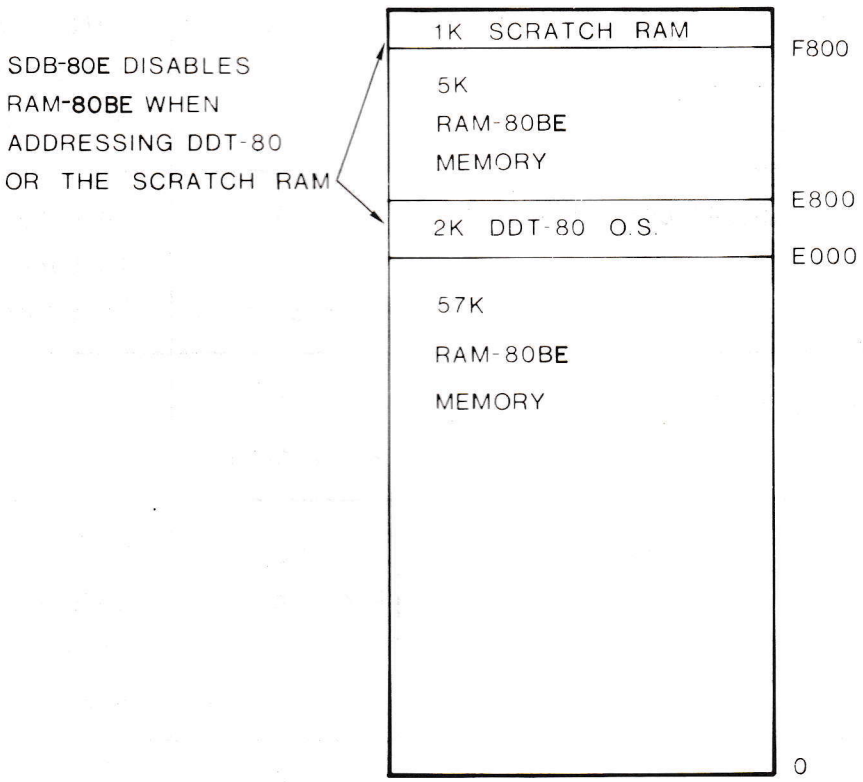


Table 3-7. Expanding RAM-80BE Memory

LOCATION	INSTALL DEVICES	INSTALL JUMPER	NOTES
0-3FFF	U36,U37,U38,U39,U40,U41,U42,U43	U3 Pin 4 to 13	Do not install unless memory disable signals are utilized.
4000-7FFF	U44,U45,U46,U47,U48,U49,U50,U51	U3 Pin 3 to 14	Shipped from factory in this configuration.
8000-BFFF	U52,U53,U54,U55,U56,U57,U58,U59	U3 Pin 2 to 15	
C000-FFFF	U60,U61,U62,U63,U64,U65,U66,U67	U3 Pin 1 to 16	Do not install unless memory disable signals are utilized.

APPENDIX A

FACTORY NOTICES

FACTORY REPAIR SERVICE

In the event that difficulty is encountered with this unit, it may be returned directly to MOSTEK for repair. This service will be provided free of charge if the unit is returned within the warranty period. However, units which have been modified or abused in any way will not be accepted for service, or will be repaired at the owner's expense. When returning a circuit board, place it inside the conductive plastic bag in which it was delivered to protect the MOS devices from electrostatic discharge. THE CIRCUIT BOARD MUST NEVER BE PLACED IN CONTACT WITH SYTROFOAM MATERIAL. Enclose a letter containing the following information with the returned circuit board:

Name, address, and phone number of purchaser
Data and place of purchase
Brief description of the difficulty

Mail a copy of this letter SEPARATELY to:

In USA:

MOSTEK Corporation
Microcomputer Service Manager
1215 West Crosby Road
Carrollton TX, 75006

OUTSIDE USA:

Please address the letter and board to the Mostek office or representtive in your country.

Securely package and mail the circuit board, prepaid and insured, to the same address.

LIMITED WARRANTY

MOSTEK warrants this product against defective materials and workmanship for a period of 90 days. This warranty does not apply to any product that has been subjected to misuse, accident, improper installation, improper application, or improper operation, nor does it apply to any product that has been repaired or altered by other than an authorized factory representative.

There are no warranties which extend beyond those herein specifically given.

NOTICE

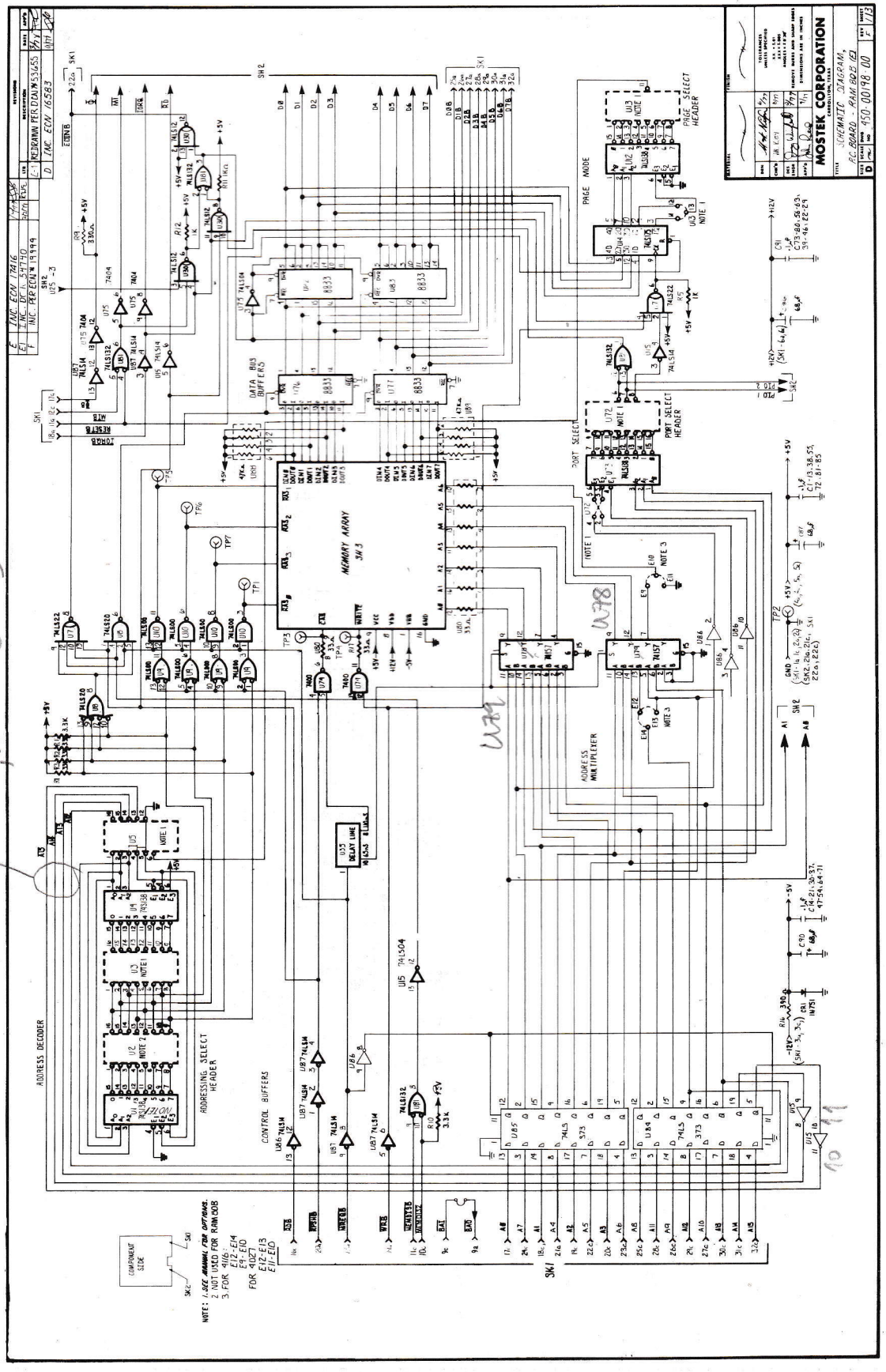
This antistatic bag is provided for shipment of the Mostek PC boards to prevent damage to the components due to electrostatic discharge.

Failure to use this bag is shipment will **VOID** the warranty.

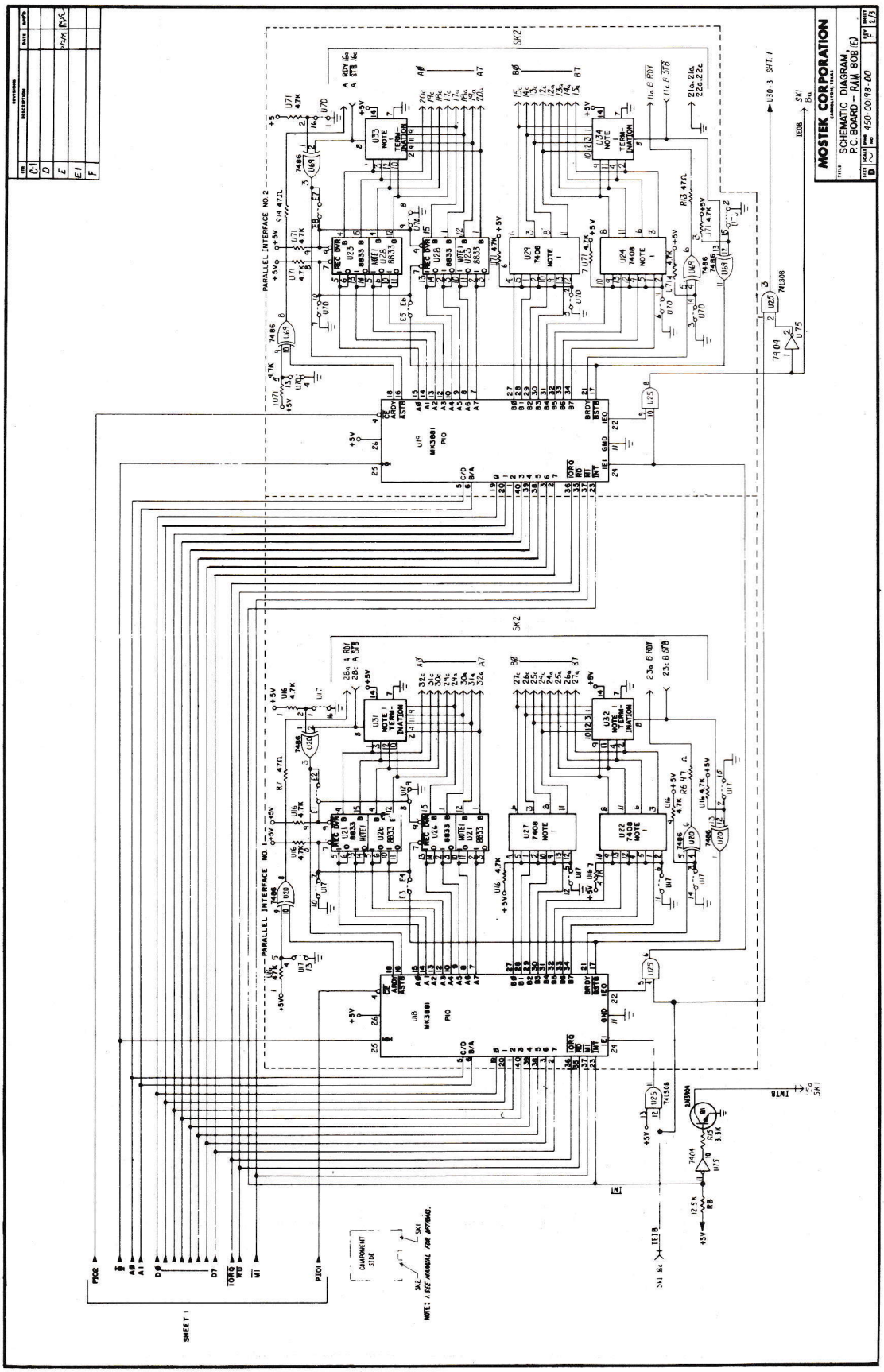
APPENDIX B

SCHEMATIC DIAGRAMS

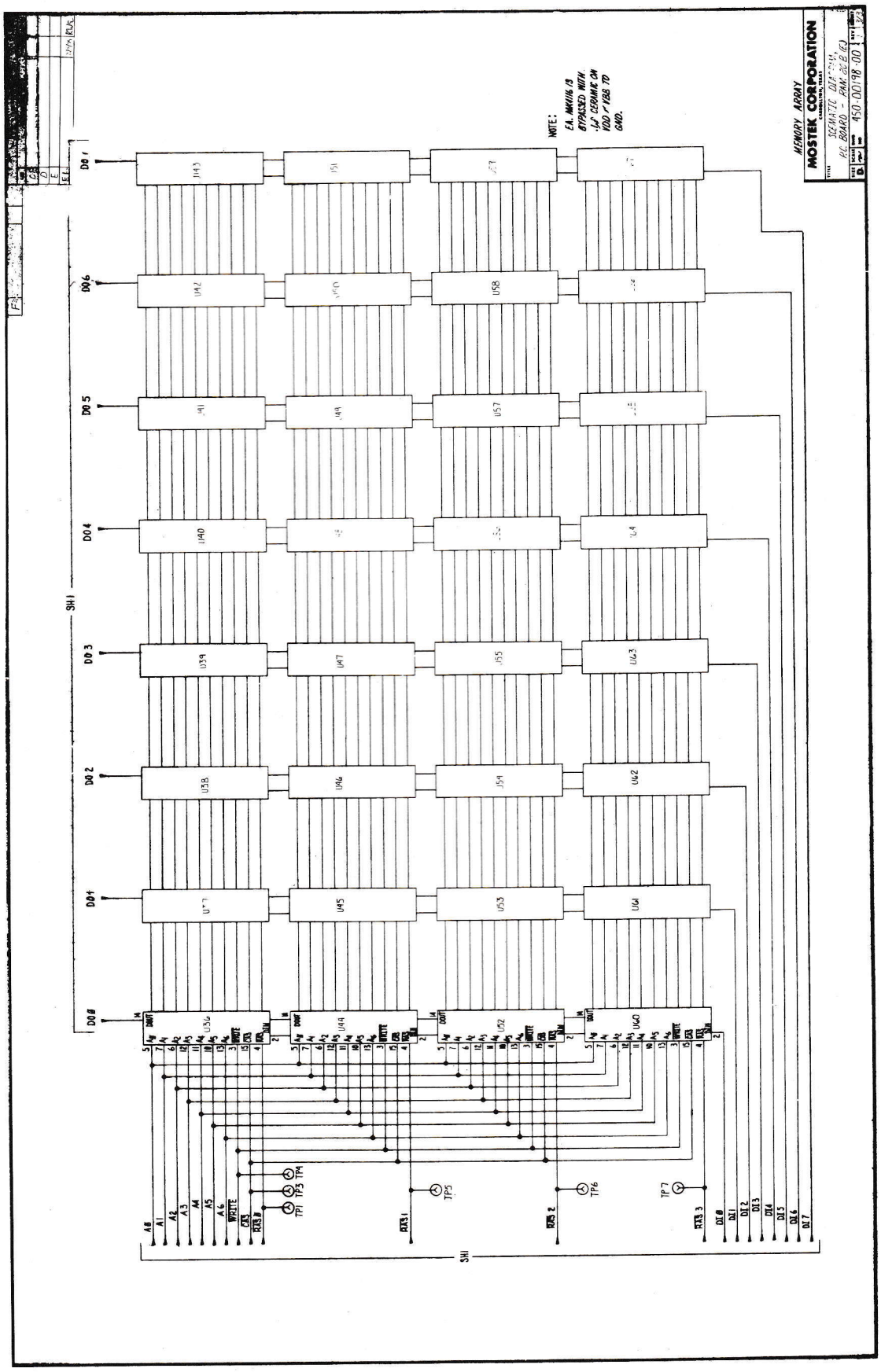
RAM-80BE Schematic Diagram (Sheet 1)



RAM-80BE Schematic Diagram (Sheet 2)



RAM-80BE Schematic Diagram (Sheet 3)

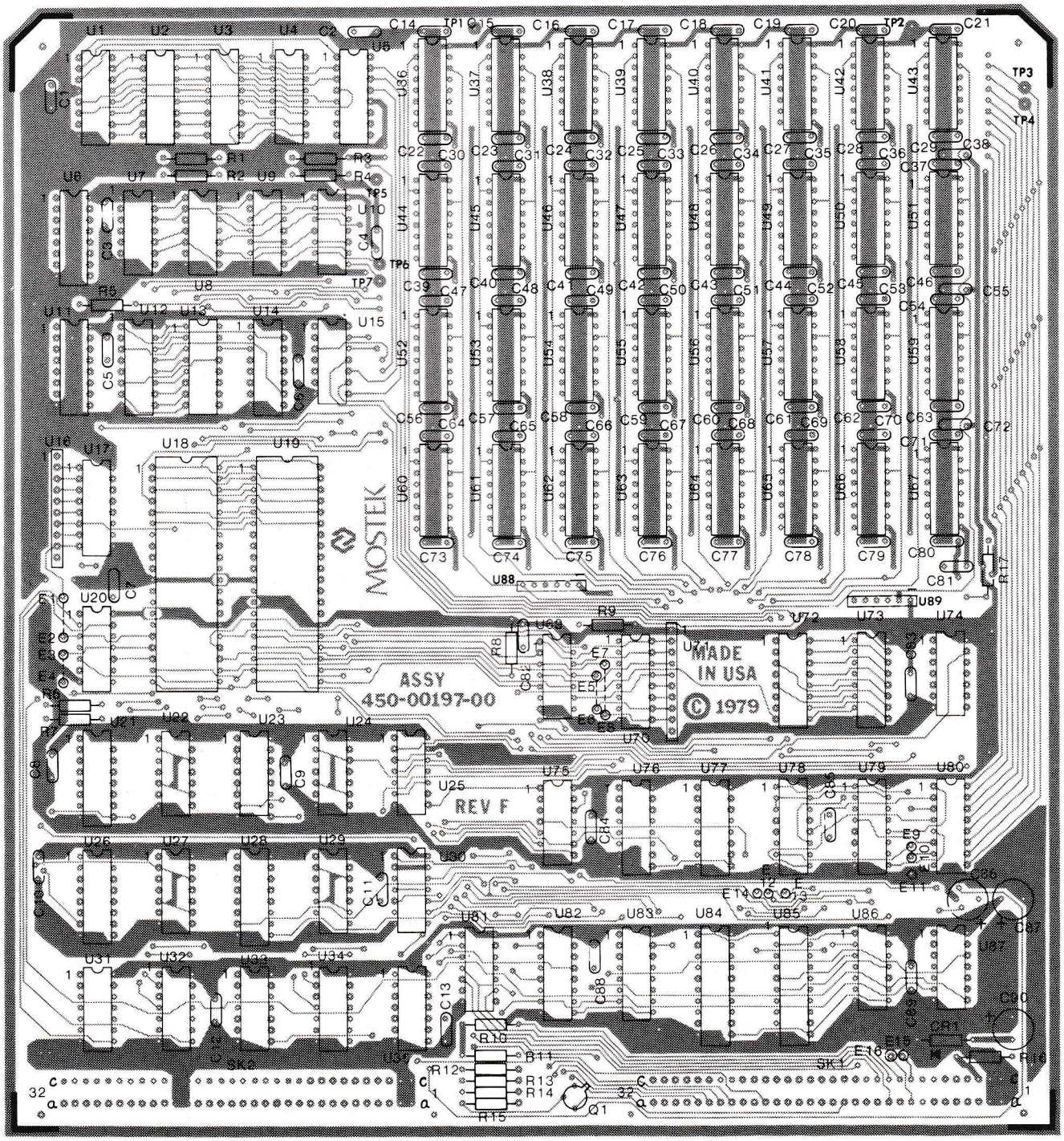


APPENDIX C

ASSEMBLY DRAWING

PARTS LIST

RAM-80BE ASSEMBLY DIAGRAM



RAM-80BE PARTS LIST

ITEM	QTY.	PART NO.	DESCRIPTION	REF. DESIG.	NOTES
44	2	4620019	SOCKET 40 PIN	X18, 19	
43	21	4280007	STAKE PINS	E1-14, TP1-7	
42	1	4470183	DIP 16 PIN 33Ω SERIES	U80	
41	4	4470176	DIP 14 PIN 1K PULL-UPS	U31-34	
40	2	4470202	SIP 6 PIN 4.7K	U88, 89	
39	2	4470175	SIP 10 PIN 4.7K	U16, 71	
38	8	4313280	16K MEMORY MK 4116	U44-51	
37	1	4313286	DELAY LINE, 110 NS	U35	
36	6	4620060	ADAPTER 16 PIN	U3.5.13.17.70.72	SEE TABLE
35	2	4140003	CARD EJECTOR		
34	2	4210057	CONNECTOR, EURO	SK1, 2	
33	1	4480047	DIODE, ZENER IN751	CR1	
32	1	4480010	TRANS. NPN 2N3904	Q1	
31	8	4620016	SOCKET 14 PIN	X22.24.27.29	
				31-34	
30	42	4620017	SOCKET 16 PIN	X3.5.13.17.21,	
				23.26, 28.	
				36-67, 70, 72	
29	3	4150114	CAP. 68μF ELECTROLYTIC	C86. 87. 90	
28	87	4150111	CAP. .1μF CERAMIC	C1-85, 88, 89	
27	1	4470057	RES. 1/4W, 33Ω, 5%	R17	
26	1	4470063	RES. 1/4W, 390Ω, 5%	R16	
25	1	4470061	RES. 1/4W, 330Ω, 5%	R9	
24	1	4470099	RES. 1/4W, 12K, 5%	R8	
23	4	4470041	RES. 1/4W, 47Ω, 5%	R6, 7, 13, 14	
22	3	4470073	RES. 1/4W, 1K, 5%	R5, 11, 12	
21	6	4470085	RES. 1/4W, 3.3K, 5%	R1-4, 10, 15	
20	4	4313291	I.C. 74LS14	U84.85.86.87	
19	1	4313294	I.C. 74LS132	U81	
18	2	4313080	I.C. 74157	U78.79	
17	1	4313006	I.C. 7404	U75	
16	1	4313002	I.C. 7400	U74	
15	1	4313290	I.C. 74LS12	U30	
14	1	4313289	I.C. 74LS08	U25	
13	4	4313010	I.C. 7408	U22.24.27.29	
12	8	4313260	I.C. 8833	U21.26.23.28	
				76.77.82.83	
11	2	4313035	I.C. 7486	U20.69	
10	2	4313270	I.C. MK 3881N	U18.19	
9	1	4313288	I.C. 74LS04	U15	
8	1	4313306	I.C. 74LS175	U14	
7	2	4313296	I.C. 74LS138	U12, 73	
6	2	4313287	I.C. 74LS00	U9, 10	
5	1	4313292	I.C. 74LS20	U8	
4	1	4313293	I.C. 74LS22	U7	
3	1	4313295	I.C. 74S138	U4	
2	1	4610041	P.C. BD. FAB (450-00196-00)		
1	REF	450-00198-00	SCHEMATIC		

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